AND8195/D

Board Mounting Notes for SO8-Flat Lead

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APPLICATION NOTE

INTRODUCTION

Various ON Semiconductor devices are packaged in an advanced power leadless package named Quad Flat No−Lead (QFN) Package. The power QFN platform represents the latest in surface mount packaging technology. It is important that the design of the Printed Circuit Board (PCB) and the assembly process follow the suggested guidelines outlined in this document.

SO8FL Package Overview

The SO8FL package was created to allow a larger MOSFET die to fit into a standard SO8IC footprint. This package uses a lead frame design that allows the leads to stick out beyond the molded body size. This feature allows the customer to see the solder fillet during visual inspection. See Figure 1 below.

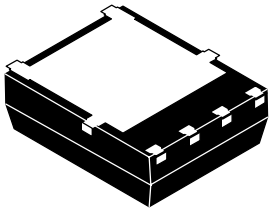

Figure 1. The Underside of an SO8FL Package

Figure 2 illustrates how the package height is reduced to a minimum by having both die and wire bond pads on the same plane. When mounted, the leads and the body are directly attached to the board without a space−consuming standoff which is inherent in a leaded package.

Figure 2 also illustrates how the ends of the leads go past the edge of the molded package. This configuration allows for the maximum die size within a given footprint, which in turn maximize the board space utilization.

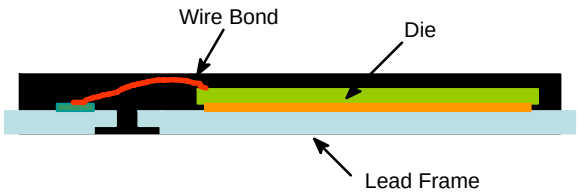

Figure 2. Cross−Section of SO8FL Package

In addition to these features, the SO8FL package has excellent thermal dissipation and reduced electrical parasitic elements due to its efficient and compact design.

Printed Circuit Board Design Considerations

SMD and NSMD Pad Configurations

There are two different types of PCB pad configurations commonly used for surface mount QFN style packages. These different I/O configurations are:

1. Non Solder Masked Defined (NSMD)
2. Solder Masked Defined (SMD)

As their titles describe, the NSMD contact pads have the solder mask pulled away from the solderable metallization, while the SMD pads have the solder mask over the edge of the metallization, as shown in Figure 3. With the SMD pads, the solder mask restricts the flow of solder paste to the top of the metallization preventing the solder from flowing along the sides of the metal pad. This is different from the NSMD configuration where the solder will flow around both the top and the sides of the metallization.

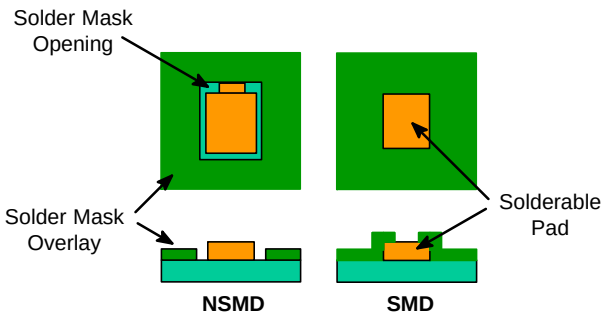

Figure 3. Comparison of NSMD vs. SMD Pads

Typically, the NSMD pads are preferred over the SMD configuration since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of a tighter tolerance than the solder masking process.

In addition, the SMD pads will inherently create a stress concentration point where the solder wets to the pad on top of the lead. This stress concentration point is eliminated when the solder is allowed to flow down the sides of the leads in the NSMD configuration.

NSMD Pad Configurations

When it is dimensionally possible, the solder mask should be located at least ±0.076 mm (0.003 in) away from the edge of the solderable pad. This spacing is used to compensate for the registration tolerances of the solder mask, as well as to insure that the solder is not inhibited by the mask as it reflows along the sides of the metal pad.

The dimensions of the PCB's solderable pads should be larger than the device footprint to allow for visual inspection of solder filet. This is shown in Figure 4. The ratio between the package's pad configuration, and that of the PCB's, is designed for optimal placement accuracy and reliability.

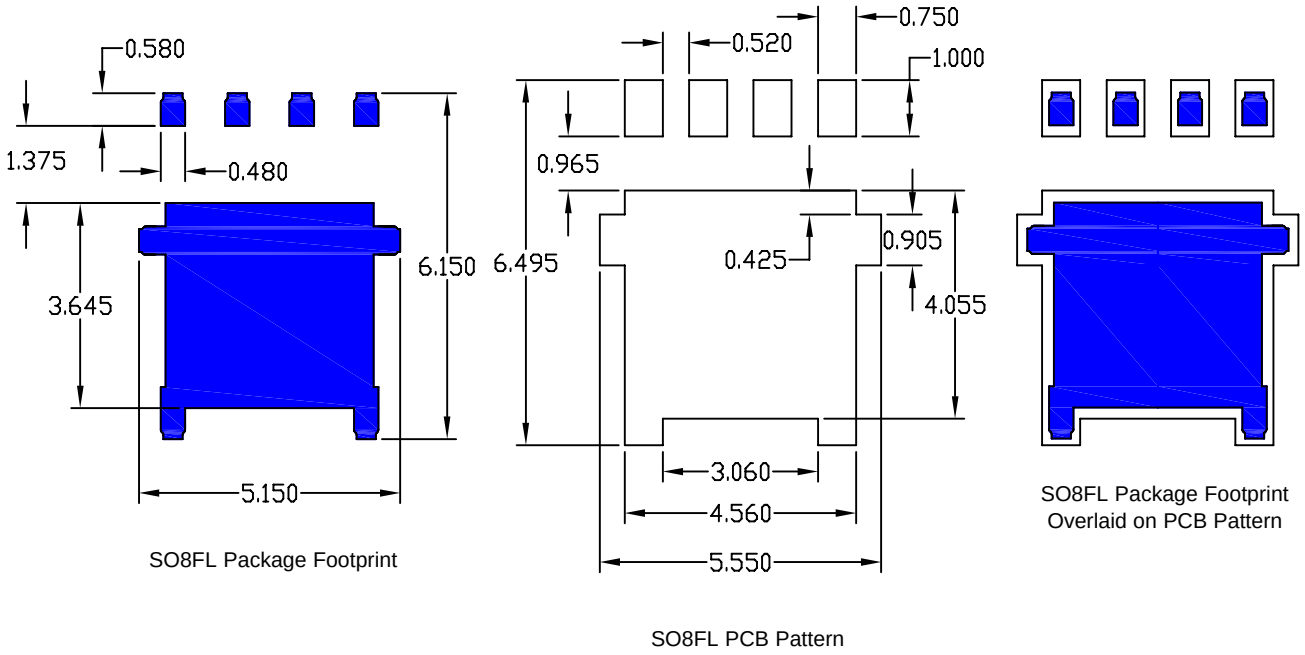

Figure 4. Printed Circuit Board Layout Using Non−Solder Masked Defined I/O Pads

SO8FL Board Mounting Process

The surface mount process is optimized by first defining and controlling the following processes:

1. Creating and maintaining a solderable metallization on the PCB contacts.
2. Choosing the proper solder paste.
3. Screening/stenciling the solder paste onto the PCB.
4. Placing the package onto the PCB.
5. Reflowing the solder paste.
6. Final solder joint inspection.

Recommendations for each of these processes are located below.

PCB Solderable Metallization

There are two common plated solderable metallization finishes which are used for PCB surface mount devices. In either case, it is imperative that the plating is uniform, conforming, and free of impurities to insure a consistent solderable system.

The first metallization finish consists of an Organic Solderability Preservative (OSP) coating over the copper plated pad. The organic coating assists in reducing oxidation in order to preserve the copper metallization for soldering.

The second recommended solderable metallization finish consists of plated electroless nickel over the copper pad, followed by immersion gold. The thickness of the electroless nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. Even though the gold metallization is typically a self−limiting process, the thickness should be of at least 0.05 μm thick, and not consist of more than 5% of the overall solder volume. Having excessive gold in the solder joint, can create gold embitterment, which may affect the reliability of the joint.

Solder Type

Solder paste such as Cookson Electronics' P/N WS3060 with a Type 3 or smaller sphere size is recommended. The WS3060 has a water−soluble flux for cleaning. Cookson Electronics' P/N C0106A can be used if a no−clean flux is preferred.

For lead free solders Sn−Ag−Cu, the following alloy (Sn 94.5%, Ag 4.5%, Cu .5%) paste is preferred.

Solder Screening onto the PCB

Stencil screening the solder onto the PCB board is commonly used in the industry. The recommended stencil thickness used is 0.075 mm to 0.127 mm (0.003 in to 0.005 in) and the sidewalls of the stencil openings should be tapered approximately 5° to facilitate the release of the paste when the stencil is removed from the PCB.

For a typical edge PCB terminal pad, the stencil opening should be the same size as the PCB mounting pad. However, in cases where the device pad is soldered to the PCB, the stencil opening must be divided into smaller cavities as shown in Figure 5. Dividing the larger pads into smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal pads to be at the same height as the larger ones. Typical solder coverage is 60 to 80% of exposed pad area.

Package Placement onto the PCB

Pick and place equipment with the standard tolerance of ±0.05 mm or better is recommended. The package will tend to center itself and correct for slight placement errors during the reflow process due to the surface tension of the solder.

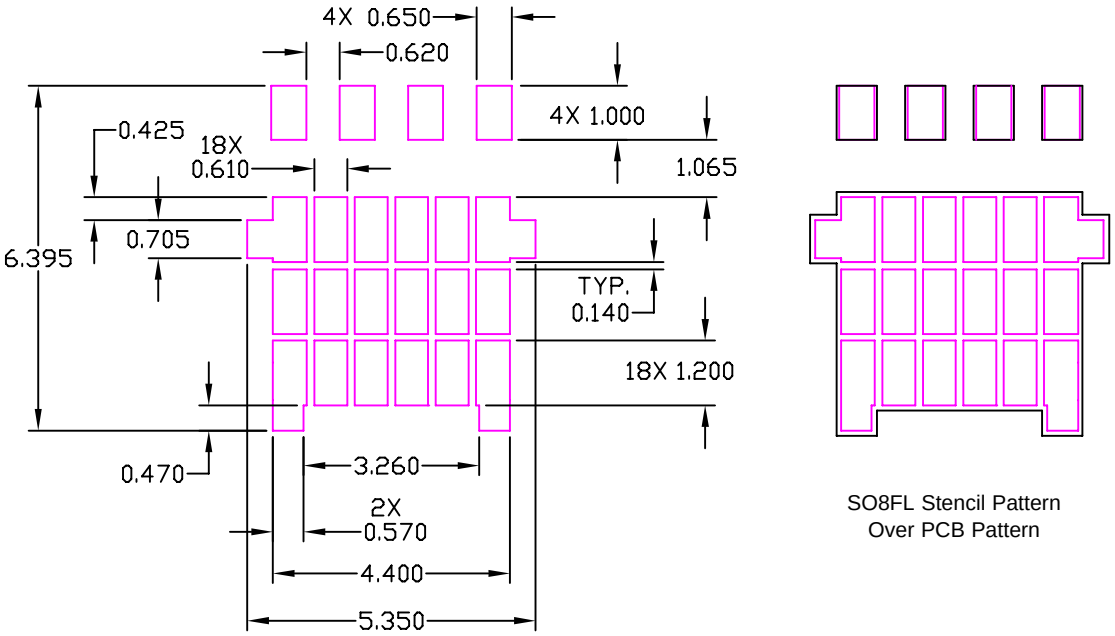

Figure 5. Solder stencil design illustrating how stencil openings are divided into an array for large die pads.

Solder Reflow

Once the package is placed on the PC board along with the solder paste, a standard surface mount reflow process can be used to mount the part. Figures 6 and 7 are examples of standard reflow profiles for typical Tin/Lead solder and Lead−free solder alloys. Note the S08FL is qualified to meet Pb−free profile requirements per JEDEC Specification J−STD−020C.

A recommended profile is available by the manufacturer of the paste since the chemistry and viscosity of the flux matrix will vary. The exact profile will be determined by the Process Engineer based on board density and thickness. These variations will require small changes in the profile in order to achieve an optimized process.

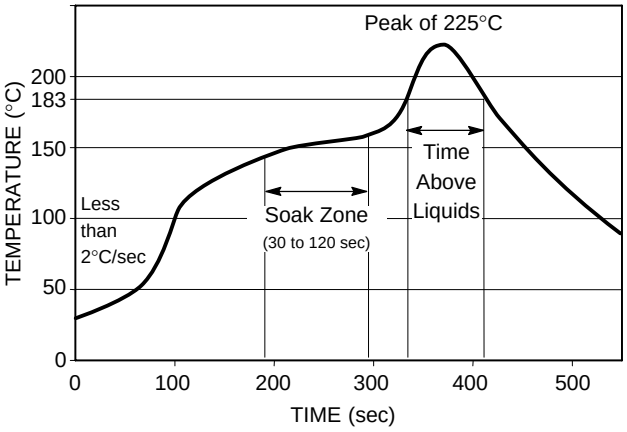

Figure 6. Typical Reflow Profile for Standard Tin/Lead Solder

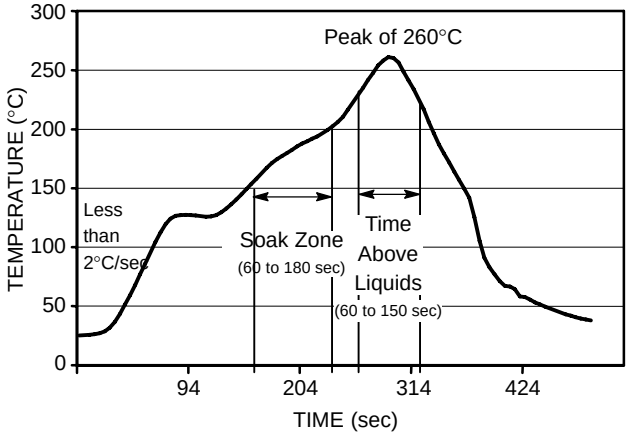

Figure 7. Typical Reflow Profile for Standard Pb−Free Solder

In general, the temperature of the part should be raised not more than 25C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 1505C and should last for 60 to 180 seconds for Pb−free profiles (30−120 sec for SnPb profiles). Typically, extending the time in the soak zone will reduce the risk of voiding within the solder. The temperature is then raised and will be above the liquidus of the solder for 60 to 150 seconds for Pb−free profiles (30−100 sec for SnPb profiles) depending on the mass of the board. The peak temperature of the profile should be between 245 and 2605C for Pb−free solder alloys (205−2255C for SnPb solders).

If required, removal of the residual solder flux can be completed by using the recommended procedures set forth by the flux manufacturer.

Final Solder Inspection

The inspection of the solder joints is commonly performed with the use of an X−ray inspection system. With this tool, one can locate defects such as shorts between pads, open contacts, voids within the solder as well as any extraneous solder.

In addition to searching for defects, the mounted device should be rotated on its side to inspect the sides of the solder joints with an X−ray inspection system. The solder joints should have enough solder volume with the proper stand−off height so that an “Hour Glass” shaped connection is not formed as shown below in Figure 7. “Hour Glass” solder joints are a reliability concern and must be avoided.

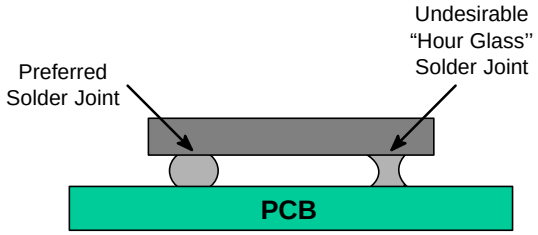

Figure 8. Side view of QFN attachment illustrating preferred and undesirable solder joint shapes

Rework Procedure

Due to the fact that the SO8FL is a leadless device, the entire package must be removed from the PC board if there is an issue with the solder joints. It is important to minimize the chance of overheating neighboring devices during the removal of the package since the devices are typically in close proximity with each other.

Standard SMT rework systems are recommended for this procedure since the airflow and temperature gradients can be carefully controlled. It is also recommended to place the PC board in an oven at 125°C for 4 to 8 hours prior to heating the parts to remove excess moisture from the packages. In order to control the region which will be exposed to reflow temperatures, the board should be heated to 100°C by conduction through the backside of the board in the location of the SO8FL. Typically, heating nozzles are then used, to increase the temperature locally.

Once the SO8FL solder joints are heated above their liquidus temperature, the package is quickly removed and the pads on the PC board need to be cleaned. The cleaning of the pads is typically performed with a blade−style conductive tool and with a de−soldering braid. A no−clean flux is used during this process in order to simplify the procedure.

Solder paste is then deposited or screened onto the site in preparation of mounting a new device. Due to the close proximity of the neighboring packages in most PC board configurations, a miniature stencil for the individual component is typically required. The same stencil design that was originally used to mount the package can be applied to the mini−stencil for redressing the pad.

Due to the small pad configurations of the SO8FL, and since the pads are on the underside of the package, a manual pick and place procedure without the aid of magnification is not recommended. A dual image optical system where the underside of the package can be aligned to the PC board should be used instead.

Reflowing the component onto the board can be accomplished by either passing the board through the original reflow profile, or by selectively heating the SO8FL with the same process that was used to remove it. The benefit with subjecting the entire board to a second reflow is that the SO8FL will be mounted consistently and by a profile that is already defined. The disadvantage is that all of the other devices mounted with the same solder type will be reflowed for a second time. If subjecting all of the parts to a second is either a concern or unacceptable for a specific application, than the localized reflow option would be the recommended procedure.

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